CONCLUSION

Applicants respectfully submit the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Robert B. O'Rourke at (408) 720-8300.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

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Date: 12/9/02

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CLAIM AMENDMENTS SHOWING CHANGES

The following is a list of all claims including claims that have not been amended in the present response To Office Action.

Please amend claims 1, 3, 6 and 10.

1. (Once amended) In a method for designing a circuit where design parameters for performance specifications are represented by posynomial expressions with constraints and solved with geometric programming, an improvement for simultaneously determining the boundaries for circuit elements in the floorplan of the circuit comprising:

representing the boundaries for circuit elements in the floorplan of the circuit as posynomial expressions with constraints on circuit size;

simultaneously solving the posynomial expressions for the design parameters and solving the posynomial expressions for the floorplan boundaries on a digital computer using geometric programming;

outputting the results in a format that can be used by a circuit designer in the fabrication of the circuit.

2. The method defined by claims 1 wherein the representation of the floorplan of the circuit includes the slicing of the circuit along the boundaries of the circuit elements.

3. (once amended) The method defined by claim 1 [or 2] including using layout constraints for the floorplan.

4. The method defined by claim 3 wherein one layout constraint is a limitation on the circuit area.

5. The method defined by claim 4 wherein another layout constraint is a limitation on the aspect ratio of the circuit layout.

6. (Once amended) In a method for designing an analog integrated circuit having active circuit elements where design parameters for performance specifications are represented by posynomial expressions with constraints and then solved with geometric programming, an improvement for simultaneously determining the boundaries for the active circuit elements in a floorplan for the integrated circuit comprising:

representing the floorplan as posynomial constraints of vertical and horizontal dimensions for regions where [each of] the active circuit elements are placed;

simultaneously solving the posynomial expressions for the design parameters and the posynomial constraints for the vertical and horizontal dimensions; and

outputting the results of the preceding step in a format usable for a circuit designer to fabricate the integrated circuit.

7. The method defined by claim 6 wherein the integrated circuit is sliced vertically and horizontally along the boundaries of the circuit elements.

8. The method defined by claim 7 wherein for a vertical slice, the resulting first sibling nodes are represented by a sum of horizontal dimensions of the first sibling nodes being equal to or less than a first parent node and which

dimensions of the first sibling nodes each being equal to or less than a vertical dimension of the first parent node.

9. The method defined by claim 8 wherein for each horizontal slice, the resulting second sibling nodes are represented by the sum of the vertical dimensions of the second sibling nodes being equal to or less than a second parent node, and the horizontal dimensions of second sibling nodes each being equal to or less than a vertical height of the second parent node.

10. (once amended) The method defined by claim [6 or] 9 wherein the circuit elements include MOS transistors where the vertical dimension and horizontal dimension of each of the MOS transistors is represented by a posynomial expression.

11. The method defined by claim 10 wherein the posynomial expression for the vertical and horizontal dimensions of the MOS transistors include process dependant parameters.

12. The method defined by claim defined by claim 11 wherein the design of the analog circuit presupposes that the active circuit elements are operating in their saturation regions.

Please add new claims 13 through 24.

13. (new) A machine readable medium having stored thereon instructions which when executed by a processor cause the processor to perform in a method for designing a circuit where design parameters for performance

specifications are represented by posynomial expressions with constraints and solved with geometric programming and for simultaneously determining the boundaries for circuit elements in the floorplan of the circuit, the method comprising:

simultaneously solving the posynomial expressions for the design parameters of the circuit and solving posynomial expressions for the floorplan boundaries of the circuit elements using geometric programming, the posynomial expressions for the floorplan boundaries represented as constraints on circuit size;

outputting the results in a format that can be used by a circuit designer in the fabrication of the circuit.

14. (new) The machine readable medium defined by claims 13 wherein the representation of the floorplan of the circuit includes the slicing of the circuit along the boundaries of the circuit elements.

15. (new) The machine readable medium defined by claim 13 including using layout constraints for the floorplan.

16. (new) The machine readable medium defined by claim 15 wherein one layout constraint is a limitation on the circuit area.

17. (new) The machine readable medium defined by claim 16 wherein another layout constraint is a limitation on the aspect ratio of the circuit layout.

18. (new) A machine readable medium having stored thereon instructions which when executed by a processor cause the processor to perform

a method for designing an analog integrated circuit having active circuit elements where design parameters for performance specifications are represented by posynomial expressions with constraints and then solved with geometric programming, and for simultaneously determining the boundaries for the active circuit elements in a floorplan for the integrated circuit, the method comprising:

representing the floorplan as posynomial constraints of vertical and horizontal dimensions for regions where the active circuit elements are placed;

simultaneously solving the posynomial expressions for the design parameters and the posynomial constraints for the vertical and horizontal dimensions; and

outputting the results of the preceding step in a format usable for a circuit designer to fabricate the integrated circuit.

19. (new) The machine readable medium defined by claim 18 wherein the integrated circuit is sliced vertically and horizontally along the boundaries of the circuit elements.

20. (new) The machine readable medium defined by claim 19 wherein for a vertical slice, the resulting first sibling nodes are represented by a sum of horizontal dimensions of the first sibling nodes being equal to or less than a first parent node and which dimensions of the first sibling nodes each being equal to or less than a vertical dimension of the first parent node.

21. (new) The machine readable medium defined by claim 8 wherein for each horizontal slice, the resulting second sibling nodes are represented by the sum of the vertical dimensions of the second sibling nodes being equal to or less than a second parent node, and the horizontal dimensions of second sibling

nodes each being equal to or less than a vertical height of the second parent node.

22. (new) The machine readable medium defined by claim 18 wherein the circuit elements include MOS transistors where the vertical dimension and horizontal dimension of each of the MOS transistors is represented by a posynomial expression.

23. (new) The machine readable medium defined by claim 10 wherein the posynomial expression for the vertical and horizontal dimensions of the MOS transistors include process dependant parameters.

24. (new) The machine readable medium defined by claim 11 wherein the design of the analog circuit presupposes that the active circuit elements are operating in their saturation regions.